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**Email for registrations**  
[jntu\\_workshop@synopsys.com](mailto:jntu_workshop@synopsys.com)

### Registration Form

## Low Power VLSI Design Methodologies - 2009 11<sup>th</sup> - 12<sup>th</sup> December, 2009

1. Name :
2. Designation :
3. Qualification :
4. Specialization :
5. Postal Address :
6. Contact Details :  
Office :  
Mobile :  
Email Id :
7. Academic Qualification :
8. Experience in Teaching / Industry :

Signature :

Date :

Signature of Sponsoring Authority.

**Last Date For Receipt Of  
Registration Form  
8<sup>th</sup> December 2009**

### A Two-Day Workshop on

## " Low Power VLSI Design Methodologies-2009"

**11<sup>th</sup> - 12<sup>th</sup> December 2009**

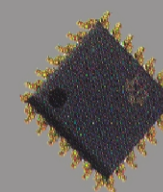
Jointly Organized by

**Synopsys (India) Pvt. Ltd.  
Hyderabad.**

# SYNOPSYS<sup>®</sup>

&

**Center for Excellence in VLSI &  
Embedded System Design (CVED)**



# CVED

J N T U H

**JNTUH COLLEGE OF ENGINEERING**  
HYDERABAD-500085, ANDHRA PRADESH

Co-ordinators

**Dr. M. Madhavi Latha  
Dr. M. Asha Rani  
P.B.V. Vasantha Kumar**

**Jawaharlal Nehru Technological University**, the First Technological University of India, was established on 2<sup>nd</sup> October 1972 in Andhra Pradesh with head quarters located in a historical city Hyderabad. The University is one of the premier Universities in India accredited by NAAC with 'A' Grade. After successful and proven levels of appreciated existence and stature spanning over 36 years. JNTU has been divided into four different universities by Govt. of Andhra Pradesh, through Act No. 30, Dt. 24<sup>th</sup> September, 2008. One of the constituent colleges of the University "**JNTUH College of Engineering, Hyderabad**" is regarded as a pioneer in shaping the excellence of some of the leading organizations of the industry, by churning out the finest professionals with a resolve to scale greater heights in the technological scenario, every year. Other constituent college of JNTUH is located at Jagityal and 11 other academic units at Hyderabad campus.

The **Center for Excellence in VLSI and Embedded System Design (CVED)**, is established in July 2009 in JNTUH, aimed at creating the necessary infrastructure facilities for carrying out the studies and investigations in identified R&D areas, related to VLSI Design, Embedded Systems Design, Development and Testing.

### SYNOPSYS

Synopsys is a world leader in electronic design automation (EDA), supplying the global electronic market with the software, IP and services used in semiconductor design and manufacturing. Synopsys comprehensive, integrated of implementation, verification, IP, manufacturing and FPGA solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India.

### About the Workshop:

Low power VLSI Technology is one of the emerging fields in rapidly growing today's technology. Because of the rising popularity of Low Power in VLSI, it is intended to create awareness of present scenario. The workshop will provide the opportunities to flourish the knowledge and to pursue research in this area.

### Topics to be covered :

- Low Power VLSI Challenges and Requirements
- Low Power Design Methodology
- Low Power Implementation Challenges
- Low Power Verification
- Hands on experience on Low Power Design using Synopsys Tools.

### Faculty :

Faculties are drawn from Synopsys (India) Pvt. Ltd., Hyderabad, India

### Eligibility :

Faculties of Educational Institutions / Graduate Engineers / Research Scholars / Research Personnel working in R&D Organization, with minimum qualification of Bachelor's degree in Electronics & Communication / Electrical / Computer Science and allied branches of Engineering, are eligible to apply.

### Important Dates :

Last date for registration : **8<sup>th</sup> December 2009**

### How to apply :

Interested persons may send an e-mail to ([jntu\\_workshop@synopsys.com](mailto:jntu_workshop@synopsys.com)) on or before 8<sup>th</sup> December '2009. Participants need to submit a letter from Sponsoring College Principal on 11<sup>th</sup> December '2009.

### Workshop timings :

**11<sup>th</sup> December 2009, 8.30 a.m. to 5.30p.m.**

**12<sup>th</sup> December 2009, 9.00 a.m. to 5.30p.m.**

## Workshop

**will be conducted at**

**Synopsys (India) Pvt. Ltd.**

**My Home Tycoon,**

**4th Floor, Block 'A',**

**Begumpet, Hyderabad.**